MEET UDESHI

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Research interests: hardware security, reverse engineering, decompilation

EDUCTATION

PhD, Electrical Engineering, New York University Sep'22 - Present
CRRL + CCS, Advisors: Prof. Farshad Khorrami and Prof. Ramesh Karri

- Research focus on reverse engineering of cyber-physical systems
- CPGA: 4.00 / 4.00

Dual Degree B.Tech + M.Tech, Electrical Engineering, IIT Bombay Jul'14 - Jun'19
Advisor: Prof. Virendra Singh

- Masters thesis focused on hardware security
- Member of Computer Architecture and Dependable Systems Lab
- CGPA: 8.18 / 10.00

PUBLICATIONS

N. K. Boran, S. Rathore, **M. Udeshi** and V. Singh, "Fine-Grained Scheduling in Heterogeneous-ISA Architectures," in IEEE Computer Architecture Letters, vol. 20, no. 1, pp. 9-12, 1 Jan.-June 2021

M. Udeshi, H. Garg, V. Baddi, P. Dwarakanath and S. Ladwa, "Low Power Object Tracking on AI100 using Kernelized Correlation Filters," in Qualcomm QBuzz Conference 2021 (won **Best Paper Award**)

ACHIEVEMENTS

Awarded the **DAC Young Fellowship** to present a poster at DAC'23

Awarded the **Recognition of Outstanding Contributions** (RoCStar) for the AI100 compiler and KCF projects

Received a **Gold Medal** in Indian National Physics Olympiad given to top 35 students across the country

Scored **Advanced Performer (AP)** grade in CS101, awarded to top 3 students in a batch of 200

RESEARCH & WORK EXPERIENCE

PhD Project - REMaQE Aug'22 - Present
Control/Robotics Research Lab, Center for Cybersecurity

- Designed REMaQE: reverse engineering math equations from binary executables
- Leveraged the **Angr symbolic execution** framework for analysis of binaries
- Devised an **automatic parameter analysis** methodology to extract input, output and constant parameters
- Implemented an **algebraic simplification** algorithm to simplify symbolic expressions
- Generated a **dataset of math equations** compiled into approx. 20,000 binaries

Senior Engineer - Qualcomm R&D Jul'19 - Jul'22
ML Compiler Team for Cloud AI100 Accelerator

- Worked on key aspects of AI100 compiler like multi-core, multi-thread and SIMD parallelization, memory management, graph scheduling and operator fusion
- Innovated various **graph optimization techniques** applicable to 2D and 3D computer vision models, recommendation systems and autonomous driving tasks
- Developing an **automatic SIMD code generation** framework for ML operators using dataflow analysis
- Contributed to the open-source **Pytorch Glow** compiler framework

- Deployed power efficient object tracking pipeline using **Kernelized Correlation Filters (KCF)** on AI100

Master's Thesis - Hardware Security Aug'18 - Jun'19
Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Designed a **prefetcher disabling attack** to amplify cache side-channel leakage which achieves **99%** reduction in prefetches generated by **AES program**
- Implemented confidence measurement for stride and DCPT prefetcher in **GEM5** simulator
- Simulated a timing attack on the **re-order buffer** using **SNIPER** x86 simulator
- Implemented **microbenchmarking tools in x86 assembly** to reverse-engineer cache information of Intel cores

R&D Project - HIDC: Heterogeneous-ISA Dynamic Core Aug'17 - Jul'18
Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Implemented abstractions which help programs running on HIDC to migrate between two ISAs during execution
- Created a stack analysis and mapping framework for x86 to ARM migrations which analyses **LLVM-IR**
- Proposed a granular function level migration strategy to reduce cost of migration by **100x**
- Benchmarked the migration time between x86 and ARM for programs from **SPEC-2006** using **GEM5** simulator

Google Summer of Code - Kivy May'16 - Aug'16
Python Native UI Framework Game Engine

- Created a **Python+Cython** module for Tiled maps integration with the **KivEnt** Game Engine
- Implemented Cython optimized **Animation System** using entity-component architecture

Software Development Intern - Amazon India Jul'17 - Aug'17
Transportation Financial Systems

- Implemented processing and sorting of **1 million+ receipts** daily using **DynamoDB, SQS**
- Automated server setup containing 30+ AWS resources in **CloudFormation**

SKILLS

Relevant Courses

Hardware Security and Trust
Advanced Computer Architecture
Advanced Hardware Design
Deep Learning

Programming

Embedded C/C++	★★★★★
Python	★★★★★
VHDL/Verilog	★★★★☆

Frameworks

Angr Symbolic Execution	★★★★★
Pytorch Glow Compiler	★★★★☆
LLVM Compiler	★★★★☆
OpenCV	★★★☆☆

Tools and Simulators

Ghidra	★★★★★
Vivado HLS	★★★★☆
Gem5	★★★★☆

OPEN SOURCE CONTRIBUTIONS

Created and maintained **Youtube Fast Playlist**, a webapp to rapidly form playlists from Youtube videos

Contributed the "merge albums" feature to the **beets** music library manager

Collected a bug bounty on bug fixes for the **Kivy Python NUI** framework

Worked on UI aspects of the **wptview** web application for **Mozilla**

Made minor contributions to the **Numpy** repository

LEADERSHIP & TEACHING POSITIONS

Mentor for a hardware security project in the Qualcomm Innovation Fellowship from Aug'20 to May'21

Teaching Assistant for VLSI Design lab in Spring'19 under Prof. Sachin Patkar

Teaching Assistant for Microprocessors course in Fall'18 under Prof. Virendra Singh

Manager of Electronics Club, IIT Bombay for Fall'16 and Spring'17 semesters

Teaching Assistant for Computer Programming flipped classroom in Summer'16 under Prof. D.B.Phatak

Reviewer in the 46th International Physics Olympiad in Jun'15

INDEPENDENT RESEARCH & ACADEMIC PROJECTS

RFID-based Secure Point-of-Sale Payment System Sep'20 - Dec'20
Swadeshi Microprocessor Challenge

- Designed a Point-Of-Sale system using the Shakti microprocessor with cryptography hardware extensions
- Developed a payment interface based on RFID cards using RFID security features
- Conceptualized a business strategy to deploy payment systems in public transport networks like Mumbai Metro

Core Team Member, Kindred Networks Jan'18 - Aug'18
Communication Services startup for IoT

- Developed an end-to-end **LoRaWAN** communication solution using **Raspberry Pi** and **STM32** platforms
- Designed custom Raspberry Pi shield with radio concentrator, GSM and GPS module
- Deployed proof-of-concept water metering project in Delhi in collaboration with Faclon Labs

Zedroid: Android on Zedboard Spring'18
VLSI Design lab, Guide: Prof. Sachin Patkar

- Rebuilt Android 5.0 OS on top of Linux Kernel v3.2 for Zynq platform
- Modified OS init procedure to enable on-board networking with **Android Debug Bridge**
- Interfaced with on-board FPGA for performance intensive applications like video-streaming

Hexapod Navigation using Local Positioning Spring'18
Embedded Systems course, Guide: Prof. Kavi Arya

- Achieved **10% location accuracy** in $2.25m^2$ area with **RSSI trilateration** for local positioning using **ZigBee**
- Designed a Hexapod with 18 degrees of freedom and implemented path-following robot using local positioning

PODEM implementation for Combinational ATPG Spring'18
VLSI Testing course, Guide: Prof. Virendra Singh

- Implemented **Path-Oriented Decision Making** for test generation of combinational circuits
- Integrated algorithm with **Deductive Fault Propagation** to boost performace
- Built logic gate test simulation framework in C++

Photoplethysmograph Sensor Fall'17
Sensors course, Guide: Prof. Siddharth Tallur

- Designed analog filters for denoising and **200x amplification** of IR sensor output
- Implemented 16-value FFT processing on **Arduino** to extract heart-rate
- Tested with 3 skin tones and illumination current of $5 - 15mA$ to quantify sensor effectiveness

EXTRA CURRICULARS

Volunteered to teach Business Studies as part of Supplemental Learning Program of **Vidya NGO**

Won third place in Case-Study competition at **Inter-IIT Tech Meet 2018** held at IIT Madras

Awarded **Tech Special Mention** by hostel for year 2015–2016 among 500+ students

Mentored 5 participants in **Kharagpur Winter of Code** to contribute to Youtube Fast Playlist